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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,868	10/06/2000	Zhaohui Shen	00-255 1496.00039	2832

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/684,868	SHEN ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Claim 1 recites a "functional portion"; therefore, the "functional portion" must be clearly shown in the drawings or the "functional portion" canceled from the claim.

Claims Objections

Claim 1 is objected to because it is not clear what being "configured" (line 4), and "said function portion" on line 5 should be changed to - - said functional portion - -.

Claim 10 is objected to because "said FPGA core" lacks antecedent basis and should be changed to - - [said] an FPGA core - -

Claim 21 is objected to because "the programmable portion" and "said plurality of signals" lack antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –
(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) The invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Killian et al (USP 6477683) who discloses a system/method comprising:

(Claim 1)

a circuit comprising a functional portion and a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said functional portion (fig 1-15).

(Claim 2) Logic potion includes one or more interfaces and said system further comprises a debugging/bug fix circuit configures to detect errors in said logic portion through said one or more interfaces (fig 1-15).

(Claim 3) diagnostic architecture using an FPGA core (c32-33) in system on a chip design (c2: 2+, c12 and/or c7: 33+, fig 2)

(Claim 4) said system is configured to provide **ease** in bringing up (this is merely an intended used and/or expected result, just for applicant information the prior art teach intended use/expected result in c11: 14+), verification (abstract/backgound/summary) and debugging (abstract/background/summary, also see fig 1- 2, 6), each by interconnecting said circuit and said debugging/bug fix circuit (fig 1-15)

(Claim 5) said system is configured to provided one or more programming options for said circuit (background/summary and/or, see flexibility/options/changes/variety/differences in code/software/programs/instructions/algorithms/tools/design/configuration in this prior art)

(Claim 6) observation of one or more signals by said debugging/bug fix circuit (fig 1-15)

(Claims 7-8) observation of one or more signals when running in a normal mode (c13: 22), single step mode (c24: 8+, c25: 63, c29: 48)

(Claims 9-11) single step mode when control by a gate or core, said core comprises [said] an FPGA core, said core is programmable (fig 1-2, 6-15, c32-33)

(Claim 12) (debugging) workstation is merely and intended use; just for the applicant information (the prior art teach an intended use; i.e., debugging computer/system/platform in fig 1 and/or c12: 31+, c26: 1-2, c30: 20+, c31: 11+, c32: 34+)

(Claims 13, 22) said debugging/bug fix circuit (and said circuit) is/are further configured to allow or more debugging features (fig 1-8 and/or c29-32)

(Claim 14) triggering and tracing based on one or more signals (c12-13, fig 2, 8)

(Claim 15) dynamically changing host register values (fig 1, c5 and/or c13-16 and/or c30-31)

(Claim 16) complex monitoring function (c2, 21)

(Claim 17) configured to reduce the debugging/verification time and/or improved product time to market is merely and intended use and/or expect result; just for the applicant information, this prior art also teach intended use and/or expected result; i.e., abstract, field of invention and/or c2, 32, 35)

(Claim 18) said circuit is further configured to operate in a normal mode (c13: 22) and a single step mode (c24: 8+, c25: 63, c29: 48)

(Claim 19) said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode in configured to provide a plurality of signals of said functional portion (fig 1-15)

(Claim 20) Scan chain is used to diagnose or fix a bug via the logic portion (c12, 21, 29, 43 and/or fig 9-15)

(Claim 21) [the] a (programmable) portion is further configured to bridge one or more of [said] a plurality of signals between a plurality of modules (fig 1-2, 6, 8)

(Claim 23) CAD software to provide one or more diagnostic functions (fig 1 and/or c12 and/or debugging/diagnostic softwares/programs/CADs/tools as taught in this reference)

(Claim 24) diagnostic function are selected from the group consisting of searching for a specific signal pattern, tracing the internal state machine, triggering on a programmed condition, and other appropriate diagnostic functions (fig 2, 6, 8 and/or c3, 5, 13, 19-20, 27, 33-34)

(Claim 25) diagnostic function are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implement statistics counting to measure the performance and the testing coverage (fig 2, 6, 8 and/or c2-4, 19-20, 23, 27, 33-34, 41-42)

(Claim 26)

(A) interfacing a chip with a core (fig 1-15)

(B) preparing one or more internal signal of said chip (fig 1-15)

(C) verifying or fixing bugs in said chip with said one or more signal (fig 1-15)

(Claim 27) a computer readable medium configured to store instruction for executing the steps of claim 26 (fig 1 and/or c12: 31+, c26: 1-2, c30: 20+, c31: 11+, c32: 34+)

2. Claims 1-3, 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Amini et al (USP 5497378) who discloses a system/method comprising:

(Claim 1)

a circuit comprising a functional portion and a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said functional portion (fig 1, 6, 11-12).

(Claims 2-3) interface and FPGA (fig 1, 6, 11-12).

(Claim 26)

(A) interfacing a chip with a core (fig 1-21)

(B) preparing one or more internal signal of said chip (fig 1-21)

(C) verifying or fixing bugs in said chip with said one or more signal (fig 1-21)

3. Claims 1-3, 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Dap et al (USP 5588152) who discloses a system/method comprising:

(Claim 1)

a circuit comprising a functional portion and a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said functional portion (fig 2, 4-6, 19).

(Claims 2-3) interface and SOC FPGA (fig 2, 4-6, 19).

(Claims 26-27)

(A) interfacing a chip with a core (fig 2, 4-6, 19);

(B) preparing one or more internal signal of said chip (fig 2, 4-6, 19);

(C) verifying or fixing bugs in said chip with said one or more signal (fig 2, 4-6, 19)

4. Claims 1-3, 26-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Winegarden et al (USP 6467009) who discloses a system/method comprising:

(Claim 1)

a circuit comprising a functional portion and a logic portion connected to said functional portion and configured to detect, fix or verify fixes of errors in said functional portion (fig 2, 11-12, 18-22, 27-30, 41-22).

(Claims 2-3) interface and SOC FPGA (fig 2, 11-12, 18-22, 27-30, 41-22).

(Claims 26-27)

(A) interfacing a chip with a core (fig 2, 11-12, 18-22, 27-30, 41-22);

(B) preparing one or more internal signal of said chip (fig 2, 11-12, 18-22, 27-30, 41-22);

(C) verifying or fixing bugs in said chip with said one or more signal (fig 2, 11-12, 18-22, 27-30, 41-22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh
Patent Examiner
June 20, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
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